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EXAMINER	
HSU, JONI	

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2671	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,936	NOONBURG, DEREK B.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 9-11, and 14-27 are rejected under 35 U.S.C. 102(e) as being anticipated by McGuinness (US006104416A).

3. With regard to Claim 1, McGuinness describes a method for generating memory requests to fetch read data from a memory (*the desired array portion is then read from memory*, Col. 3, lines 39-41; *request to access the memory*, Col. 6, lines 37-40), the memory comprising a plurality of memory pages, each of the memory pages having a plurality of words (Col. 8, lines 51-59), the method comprising the steps of determining a location of the read data in the memory (*reading data in a word having a word address*, Col. 3, lines 43-51); selecting a packetization

scheme based on the location of the read data and on fitting the read data into a plurality of data packets; and assembling at least one read command for fetching the read data from the memory in accordance with the selected packetization scheme (Col. 11, lines 10-24).

4. With regard to Claim 2, McGuinness describes the step of sending the at least one read command corresponding to the plurality of data packets to the memory (*command to access a block of N words*, Col. 8, lines 1-4).

5. With regard to Claim 3, McGuinness describes the step of fetching the read data in response to sending the at least one read command (Col. 8, lines 1-4).

6. With regard to Claim 4, McGuinness describes that the read data comprises a reference pixel chunk having a luminance chunk and a chrominance chunk (Col. 4, lines 40-52; Col. 13, lines 60-67).

7. With regard to Claim 5, McGuinness describes that the step of determining the location of the read data further comprises receiving at least a set of motion vectors pointing to the reference pixel chunk (*determines the word address in memory 180 where the frame, and the prediction block within the frame, that is needed to form the motion compensation prediction is located, these addresses are computed using the prediction modes and motion vectors*, Col. 5, lines 19-39).

8. With regard to Claim 6, McGuinness describes the step of determining a first set of components associated with the reference pixel chunk based on the at least a set of motion vectors (Col. 4, lines 40-52; Col. 5, lines 19-28).

9. With regard to Claim 7, McGuinness describes that the step of selecting a packetization scheme further comprises combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages (Col. 8, lines 51-67; *luminance Y and both chrominance Cr and Cb are stored in one 32 byte word*, Col. 10, lines 19-30).

10. With regard to Claim 9, McGuinness describes that the step of selecting a packetization scheme further comprises combining a first part of the chrominance chunk and a second part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the chrominance chunk overlaps more than one of the plurality of memory pages (Col. 8, lines 51-67; *both chrominance components are stored in one word*, Col. 9, lines 55-65).

11. With regard to Claim 10, according to the disclosure of this application, a virtual page boundary is placed to split the left 2 words of each row. Therefore, the chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create a symmetry that allows the reduction of the number of cases that need to be considered for packetization [0068]. McGuinness describes interlacing the

luminance Y and both chrominance Cr and Cb so that all of the components can be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (Col. 10, lines 26-30). Storing the chrominance components so interlaced enables the FIFO that stores the chrominance to have the same structure as the FIFO storing the luminance (Col. 10, lines 8-9), and therefore creates symmetry. Therefore, McGuinness discloses the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme.

12. With regard to Claim 11, according to the disclosure of this application, a virtual page boundary is placed to split the left 2 words of each row. Therefore, the chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create a symmetry that allows the reduction of the number of cases that need to be considered for packetization [0068]. McGuinness describes interlacing the luminance Y and both chrominance Cr and Cb so that all of the components can be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (Col. 10, lines 26-30). Storing the chrominance components so interlaced enables the FIFO that stores the chrominance to have the same structure as the FIFO storing the luminance (Col. 10, lines 8-9), and therefore creates symmetry. Therefore, McGuinness discloses the step of placing a virtual memory page boundary across the chrominance chunk, the virtual memory page boundary being associated with the packetization scheme.

13. With regard to Claim 14, McGuinness describes that each of the at least one read command (Col. 3, lines 39-41; Col. 6, lines 37-40; Col. 8, lines 1-4) includes specifications for combining selected ones of the plurality of words from selected ones of the plurality of memory pages into the plurality of data packets (Col. 8, line 51-Col. 9, line 11).

14. With regard to Claim 15, McGuinness describes that the plurality of data packets is equal to or less than a predetermined number (*the access to a portion of a picture must be decomposed into a number of atomic transfers, each involving the transfer of a certain number of bytes or words*, Col. 7, lines 55-60; *access a block of N words*, Col. 8, lines 1-12; *for a 32 word FIFO, each word being 16 bytes long, when each tile has 64 rows, a maximum of 2 bursts is required to fill the FIFO*, Col. 9, lines 7-11).

15. With regard to Claim 16, McGuinness describes that the predetermined number is a compromise between trying to keep the number of rows in a tile small enough that when the tile is stored right after the tile immediately to its left the pixels in one row of the picture are close enough to be retrieved in a reasonable number of bursts in page mode access, yet large enough to allow a prediction block to be retrieved in one to two bursts (Col. 8, lines 59-67). Therefore, the predetermined number and the selected ones of the plurality of memory pages can inherently be adjusted to any number in order to meet this compromise. Therefore, the predetermined number can be four and the selected ones of the plurality of memory pages can be two (Col. 9, lines 7-9).

16. With regard to Claim 17, McGuinness describes that the predetermined number is a compromise between trying to keep the number of rows in a tile small enough that when the tile is stored right after the tile immediately to its left the pixels in one row of the picture are close enough to be retrieved in a reasonable number of bursts in page mode access, yet large enough to allow a prediction block to be retrieved in one to two bursts (Col. 8, lines 59-67). Therefore, the predetermined number and the selected ones of the plurality of memory pages can inherently be adjusted to any number in order to meet this compromise. Therefore, the predetermined number can be four and the selected ones of the plurality of memory pages can be three.

17. With regard to Claim 18, McGuinness describes that the plurality of data packets comprise 16 words (Col. 9, lines 7-11).

18. With regard to Claim 19, McGuinness describes a method for packing read data into data packets, the read data being stored in a memory, the memory comprising a plurality of memory pages, the method comprising the steps of receiving at least one read command requesting the read data, the at least one read command comprising specifications for including in the data packets a selected portion of the read data from at least one of the plurality of memory pages; sending instructions to the memory according to the at least one read command received, the instructions relating to a manner in which the read data requested is to be obtained from the memory; receiving the read data from the memory in response to the memory receiving the instructions; and packing the read data received into the data packets according to the

specifications of each of the at least one read commands (Col. 3, lines 39-41; Col. 6, lines 37-40; Col. 8, lines 1-4, 51-67).

19. With regard to Claim 20, McGuinness describes that the read data is a reference pixel chunk comprising a luminance chunk and a chrominance chunk (Col. 4, lines 40-52; Col. 13, lines 60-67).

20. With regard to Claim 21, McGuinness describes a method for reassembling reference pixel data (Col. 5, lines 29-38) from a plurality of data packets into a luminance chunk and a chrominance chunk, comprising the steps of receiving the plurality of data packets, each data packet comprising a portion of a reference pixel chunk including the luminance chunk and the chrominance chunk; determining a packetization scheme, the packetization scheme being used to packetize the luminance and chrominance chunks into a plurality of data packets; and unpacking the plurality of data packets into a reassembled luminance chunk and a reassembled chrominance chunk based on the packetization scheme (Col. 9, line 42-Col. 10, line 30).

21. With regard to Claim 22, McGuinness describes the steps of forming prediction blocks by arranging the plurality of data packets unpacked with any information related to motion vectors, and combining blocks with associated macroblocks to form a reconstructed macroblock (Col. 5, lines 10-60).

22. With regard to Claim 23, McGuinness describes the step of writing the reconstructed macroblock to a memory; selecting a packetization scheme based on a location of read data and on fitting the read data into the plurality of data packets; and assembling at least one read command for fetching the read data from the memory in accordance with the packetization scheme selected (Col. 11, lines 10-24).

23. With regard to Claim 24, Claim 24 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

24. With regard to Claim 25, Claim 25 is similar in scope to Claim 19, and therefore is rejected under the same rationale.

25. With regard to Claim 26, Claim 26 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

26. With regard to Claim 27, Claim 27 is similar in scope to Claim 19, and therefore is rejected under the same rationale.

27. Thus, it reasonably appears that McGuinness describes or discloses every element of Claims 1-7, 9-11, and 14-27 and therefore anticipates the claims subject.

28. Claims 28, 29, 31, 32, 34, 37, 38, 40, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Bheda (US005990958A).

29. With regard to Claim 28, Bheda describes a system for decoding pictures in a compressed video bit stream (*parsing the compressed video bitstream using variable length decoding*, Col. 4, lines 46-51), comprising a memory having a plurality of memory pages (Col. 6, line 66-Col. 7, line 1) storing reference pixel data (*VRP 190 averages the forward and backward reference pixel values "on the fly" as the backward reference data is being read from the memory*, Col. 23, lines 28-30); an address generator coupled to the memory for generating memory commands for fetching the reference pixel data from the memory (Col. 23, lines 15-30); and a reference data assembly module (190, Figure 13) coupled to the address generator for receiving from the memory a plurality of data packets having a portion of the reference pixel data (Col. 23, lines 21-42).

30. With regard to Claim 29, Bheda describes that the reference pixel data comprises a luminance chunk and a chrominance chunk (Col. 23, lines 1-7, 26-30).

31. With regard to Claim 31, Bheda describes that the reference data assembly module (190, Figure 13) unpacks the plurality of data packets to transform the reference pixel data into a reassembled luminance chunk and a reassembled chrominance chunk (Col. 23, lines 1-12, 28-42).

32. With regard to Claim 32, Bheda describes that the reference data assembly module comprises a plurality of data buffers, each data buffer being configured to receive one of the plurality of data packets (*HAL 142 allocates the necessary buffer area required to store the symbol stream in system memory 14, the symbol stream is written to the allocated buffer space in system memory 14 in buffers 114a,b*, Col. 6, lines 20-23, 39-53; Col. 23, lines 49-54).

33. With regard to Claim 34, Bheda describes that the reference data assembly module comprises a plurality of data buffers for buffering a reassembled luminance chunk and a reassembled chrominance chunk (Col. 6, lines 20-23, 39-53; Col. 23, lines 1-12).

34. With regard to Claim 37, Bheda describes a memory interface unit (142, Figure 6) coupled to the memory (Col. 6, lines 20-21).

35. With regard to Claim 38, Bheda describes that the memory interface unit (142, Figure 6) further comprises a memory queue (150) for storing the generated memory commands from the address generator (*HAL 142 allocates storage for and maintains a queue data structure called Task FIFO 150*, Col. 6, line 64-Col. 7, line 17; Col. 8, lines 28-35).

36. With regard to Claim 40, Bheda describes that the memory interface unit (142, Figure 6) further comprises a sequencer for forwarding the generated memory commands to the memory to obtain the reference pixel data based on specifications (Col. 22, line 48-Col. 23, line 30).

37. With regard to Claim 41, Bheda describes that the memory interface unit further comprises a packet assembly unit for assembling the plurality of data packets of the reference pixel data obtained from the memory (Col. 22, line 48-Col. 23, lines 42).

38. Thus, it reasonably appears that Bheda describes or discloses every element of Claims 28, 29, 31, 32, 34, 37, 38, 40, and 41 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

41. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over McGuinness (US006104416A) in view of Sorin (US006631164B1).

McGuinness is relied upon for the teachings as discussed above relative to Claim 4.

However, McGuinness does not teach that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages. However, Sorin describes that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of McGuinness so that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages as suggested by Sorin because Sorin suggests that typically, motion estimation calculations are performed on the luminance values alone (Col. 1, lines 46-61).

42. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGuinness (US006104416A) in view of Levy (US005170251A).

43. With regard to Claim 12, McGuinness is relied upon for the teachings as discussed above relative to Claim 1. McGuinness describes that the packetization scheme selected maps a first set of components to a second set of components (Col. 8, lines 51-67; Col. 9, lines 55-65).

However, McGuinness does not teach selecting the packetization scheme by a table lookup. However, Levy describes selecting the packetization scheme by a table lookup (Col. 2, lines 20-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of McGuinness to include selecting the packetization scheme by a table lookup as suggested by Levy. The speed gained by using a lookup table can be significant, since retrieving a value from memory is often faster than undergoing an expensive computation. Lookup tables are well-known in the art, widely used, and can be found in many publications, such as the Wikipedia Encyclopedia.

44. With regard to Claim 13, McGuinness describes that the first set of components comprises the read data corresponding to the luminance chunk and the chrominance chunk, and the second set of components comprises the selected ones of the plurality of words (Col. 9, line 55-Col. 10, line 30).

45. Claims 30 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bheda (US005990958A) in view of McGuinness (US006104416A).

46. With regard to Claim 30, Bheda is relied upon for the teachings as discussed above relative to Claim 28.

However, Bheda does not specifically teach that the memory commands comprises specifications for combining selected portions of the reference pixel data from a selected one or more of the plurality of memory pages into at least one of the plurality of data packets. However, McGuinness describes that the memory commands comprises specifications for combining selected portions of the reference pixel data from a selected one or more of the plurality of memory pages into at least one of the plurality of data packets (Col. 5, lines 28-38; Col. 8, lines 45-67).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Bheda so that the memory commands comprises specifications for combining selected portions of the reference pixel data from a selected one or more of the plurality of memory pages into at least one of the plurality of data packets as suggested by McGuinness because McGuinness suggests the advantage of combining the pixel data in such a way that they are close enough to be retrieved in a reasonable number of bursts in page mode access, yet large enough to allow a prediction block to be retrieved in one to two bursts (Col. 8, lines 45-67).

47. With regard to Claim 39, Bheda describes a memory queue (150) for storing memory commands (Col. 6, line 64-Col. 7, line 17; Col. 8, lines 28-35).

However, Bheda does not specifically teach that at least one of the plurality of data packets includes the reference pixel data from at least two of the plurality of memory pages.

However, McGuinness describes that at least one of the plurality of data packets includes the reference pixel data (Col. 5, lines 29-38) from at least two of the plurality of memory pages (Col. 8, line 51-67). This would be obvious for the same reasons given in the rejection for Claim 30.

48. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bheda (US005990958A) in view of Levy (US005170251A).

Bheda is relied upon for the teachings as discussed above relative to Claim 28. Bheda describes that the reference data assembly module (190) comprises an additional module for reassembling the reference pixel data based on a set of motion vectors and packetization scheme used to form the plurality of data packets (Col. 23, lines 12-41).

However, Bheda does not teach a table lookup used to form the plurality of data packets. However, Levy describes a table lookup used to form the plurality of data packets (Col. 2, lines 20-30), as discussed in the rejection for Claim 12.

49. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bheda (US005990958A) in view of Kim (US006525783B1).

50. With regard to Claim 35, Bheda is relied upon for the teachings as discussed above relative to Claim 28. Bheda describes a variable length decoding module (Col. 4, lines 24-29).

However, Bheda does not specifically teach that the variable length decoding module is configured to extract a set of motion vectors corresponding to a macroblock in the compressed video bit stream. However, Kim describes a variable length decoding module (104) configured

to extract a set of motion vectors corresponding to a macroblock in the compressed video bit stream (*video decoding system including a VLD, allowing control of the processing time depending upon a video bit stream compression method*, Col. 3, lines 16-24; *macroblock address generator 114 receiving macroblock addresses from the VLD decoded data and generating addresses of data to be stored in the SDRAM; a previous motion vector decoder 115 receiving motion vector codes from the VLD decoded data and decoding motion vectors*, Col. 4, lines 41-47; *VLD 104 read the bit stream and decodes the data, among the variable length decoded data from the VLD 104, the macroblock address is output to the macroblock address generator 114, the motion vector code used for decoding a motion vector is output*, Col. 5, lines 26-35).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Bheda so that the variable length decoding module is configured to extract a set of motion vectors corresponding to a macroblock in the compressed video bit stream as suggested by Kim because Kim suggests that this is how conventional video decoders operate (Col. 1, lines 35-43) and is well-known in the art.

51. With regard to Claim 36, Bheda does not specifically teach that the variable length decoding module sends the extracted set of motion vectors to the address generator. However, Kim describes that the variable length decoding module sends the extracted set of motion vectors to the address generator (Col. 4, lines 41-47, 51-57).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Bheda so that the variable length decoding module sends the extracted set of motion vectors to the address generator as suggested by Kim because Kim

suggests that in order to generate an address of the memory necessary for motion compensation, motion vectors are needed (Col. 4, lines 41-47, 51-57).

Prior Art of Record

"Lookup table." http://en.wikipedia.org/wiki/Lookup_table.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner